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Application No. 09/922,479

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and French languages, and that I believe that the attached text is a true translation of

German application DE 100 37 794.7, filed with the German Patent Office on August 3, 2000

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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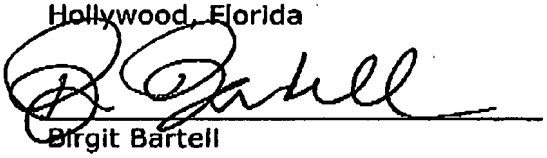

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Description

Method and device for testing an integrated circuit, integrated circuit to be tested, and wafer with a large number of integrated circuits to be tested

The present invention relates to a method according to the preamble of patent claim 1 and devices according to the preambles of patent claims 11, 16 and 24, that is to say

- a method and device for testing an integrated circuit, using a self-test device contained in the latter,

- an integrated circuit with a self-test device, and

- a wafer with a large number of integrated circuits.

Integrated circuits and methods for their production have been known for many years in an extremely wide range of embodiments.

It is likewise known that integrated circuits, semiconductor chips containing integrated circuits or components containing semiconductor chips have to be tested during or after their production.

In this case, integrated circuits which are not operating properly are repaired by deactivating the faulty parts and activating equivalent redundant parts (this is often the case, in particular, in memory modules), or - if this is not possible - are separated out.

Various possible ways of testing integrated circuits are known.

The most widespread method consists in connecting the integrated circuits still located on the wafer, or the semiconductor chips already cut out of the wafer, or the semiconductor chips already provided with a housing, to an external testing device and in testing then by supplying suitable test signals.

Additionally or alternatively, the testing of integrated circuits can also be carried out by using self-test devices which are integrated in the integrated circuits and are frequently also referred to as built-in self-test modules or BIST modules. BIST modules which operate particularly efficiently are disclosed, for example, by EP 0 492 624 A1, US 5 388 104, EP 0 568 239 A2, US 5 570 374 and by Sampath Rangarajan et al.: "Built-In Testing of Integrated Circuit Wafers", IEEE Transactions on Computers, Vol. 39, No. 2, February 1990, pages 195 ff. With the aid of such or other BIST modules, the integrated circuits can, at least to some extent, check themselves for freedom from faults.

Experience shows that the testing of integrated circuits is becoming increasingly more complicated and more costly, in spite of test methods becoming better and better and more and more efficient. The facts which are responsible for this are, in particular,

- that the clock frequency at which the integrated circuits are operated is continually increasing (this makes it increasingly more complicated to carry out the tests under the real operating conditions),

- that the clock frequency at which the integrated circuits are operated is increasing less rapidly than the number of constituents to be tested, such as the memory cells of a memory to be tested in the integrated circuit (this leads to the test time becoming increasingly longer), and

- that the number of components present in the integrated circuit is increasing sharply, while the number of input and/or output terminals on the integrated circuits is increasingly comparatively little (this leads to an increasingly more difficult and more time-consuming ability to observe the integrated circuit).

The ever more complicated and more time-consuming tests of integrated circuits have the negative effect that the testing of the integrated circuits gives rise to higher and higher costs. This is understandably a disadvantage.

The present invention is therefore based on the object of finding a possible way which permits integrated circuits to be tested rapidly and simply.

According to the invention, this object is achieved by the method and devices claimed in patent claims 1, 11, 16 and 24.

The method and devices according to the invention are defined by the fact

- that the testing of the integrated circuit by a self-test device contained therein is begun before the integrated circuit is connected to an external testing device that reads out and/or evaluates the results of the self test, or

- that the integrated circuit contains means which make it possible to arrange that, during the testing and/or after the testing of the integrated circuit by the self-test device, specific parts of the integrated circuit are taken out of operation, or

- that integrated circuits to be separated later by cutting up the wafer are at least partially electrically connected to one another.

The fact that the testing of the integrated circuit by the self-test device is begun before the integrated circuit is connected to an external testing device that reads out and/or evaluates the results of the self test means that the residence time of the integrated circuit on the external testing device can be minimal, that is to say the external testing device is therefore utilized most efficiently.

The fact

- that the integrated circuit contains means which make it possible to arrange that, during the testing and/or after the testing of the integrated circuit by the self-test device, specific parts of the integrated circuit are taken out of operation, and/or

- that integrated circuits to be separated later by cutting up the wafer are at least partially electrically connected to one another,

means that, by using a simply constructed self-test control device and simply constructed contacting devices, a large number of integrated circuits can be tested simultaneously by the self-test devices contained in them.

By means of the aforementioned method and devices, integrated circuits can consequently be tested rapidly and simply.

Advantageous developments of the invention can be taken from the subclaims, the following description and the figures.

The invention will be explained in more detail below using exemplary embodiments and with reference to the figures, in which:

figure 1 shows the construction of an integrated circuit containing a self-test device,

figure 2 shows the construction of a test result memory which is written by the self-test device and belongs to the integrated circuit according to figure 1,

figures 3A and 3B show the construction of interface circuits provided between the self-test device and the test result memory,

figure 4 shows an arrangement by means of which, after the completion of the self test, the supply voltage feed to specific parts of the integrated circuit is automatically interrupted,

figure 5 shows the waveforms of specific voltages and signals which occur during the testing of the integrated circuit according to figure 1 during the testing of the same by the self-test device,

figure 6 shows an arrangement by means of which reset signals for resetting parts of the integrated circuit are generated on

the basis of the variation in the supply voltage for the parts of the integrated circuit to be reset,

figure 7 shows a wafer carrying a large number of integrated circuits,

figure 8 shows the construction of one of the integrated circuits on the wafer according to figure 7,

figure 9 shows electrical connections via which the integrated circuits on the wafer according to figure 7 are connected to one another,

figures 10A and 10B show a wafer contacting device, by means of which contact can be made with contact points provided on the wafer according to figure 7,

figures 11A to 11C show a device by means of which a wafer lying on a carrier can be removed from the carrier without interrupting the supply of voltages or signals fed to it,

figure 12 shows a test box, in which the integrated circuits of a plurality of wafers can be tested simultaneously by the self-test devices contained in them,

figure 13 shows an arrangement in which the integrated circuits to be tested are transported on a turntable to an external testing device and, on the way there, are tested by the self-test devices contained in them,

figure 14 shows an arrangement by means of which components containing semiconductor chips can be tested efficiently, and

figures 15A and 15B show various views of a component carrier employed in the arrangement according to figure 14.

By means of the measures described in more detail below, integrated circuits may be tested rapidly and simply. The measures relate to

- the construction of the integrated circuit to be tested,

- the wafer used for the simultaneous production of a plurality of integrated circuits and, at the end, carrying a large number of integrated circuits, and also

- the method and devices for testing the integrated circuits,

it being possible for the integrated circuits to be tested particularly rapidly and simply if use is made of all the special features described. However, reference should already be made at this point to the fact that integrated circuits can be tested more rapidly and more simply than hitherto even if use is made only of individual or several of the special features described below.

The integrated circuits to be tested are, in the example considered, semiconductor circuits implemented using CMOS technology (systems on silicon), but can also be any other desired circuits; they are a constituent part of a semiconductor chip or will be further processed to form a semiconductor chip. The function of the integrated circuits to be tested is not subject to any restrictions.

The integrated circuits considered contain a self-test device, using which they can themselves test certain components or

functions. In the example considered, the self-test device is a built-in self-test module or BIST module, as it is known.

As will be described more precisely later, in response to an external request, the BIST module carries out a test of the components and functions of the integrated circuit that can be tested by it (for example of a memory contained in the integrated circuit) and writes the result of this self test into a test result memory (likewise contained in the integrated circuit). The test result stored in the test result memory is output by the integrated circuit to an external testing device when requested by the latter and is evaluated there; this external testing device in the example considered is a testing device which, in addition to evaluating the results of the self test of the integrated circuit, in addition tests those components or functions of the integrated circuit which cannot be or are not tested by the BIST module, or only partially so, by supplying suitable signals and by evaluating the reaction to these.

In the example considered, the test of the integrated circuit by the BIST module contained therein is begun before the integrated circuit is connected to the external testing device, for example as early as during temporary storage of the relevant integrated circuit and/or during the transport of the relevant integrated circuit to the external testing device; the test of the integrated circuit by the BIST module contained therein has preferably already been concluded when the integrated circuit is connected to the external testing device.

As a result, after the production of the connection to the integrated circuit to be tested, the external testing device can immediately begin

- reading out and evaluating the results of the test carried out by the BIST module, and

- testing the components and functions of the integrated circuit to be tested which are not tested by the BIST module.

Since the external testing device does not itself have to perform the initiation of the test to be carried out by the BIST module, and does not then have to wait until the end of this test before it can begin with reading out and evaluating the results of the test carried out by the BIST module and/or the continued testing of the integrated circuit to be tested, the residence time of the integrated circuit to be tested on the external testing device is minimal, and the utilization of the external testing device is optimal.

Shortening the residence time of the integrated circuit to be tested on the external testing device may appear to be unimportant. However, if one takes account of the immense number of integrated circuits which have to be tested by the external testing device over the course of time, then, even if only a fraction of a second can be saved on each integrated circuit, the result is an enormous saving in time.

The initiation and the implementation of the test to be carried out by the BIST test module without concomitant action by the external testing device does not present any kind of problems: as will be understood still better later on, for this purpose it is merely necessary to make contact with only a few terminals of the integrated circuit and to apply to them the voltages and signals needed to initiate the test; the test itself can proceed automatically (without any external control).

An integrated circuit which is particularly suitable for the above-described procedure is illustrated in figure 1. For completeness, it should be noted that, of this integrated circuit, only the BIST module, the test result memory and the constituent parts of the integrated circuit that are needed for its proper operation are shown and described.

The integrated circuit shown in figure 1 contains a self-test device in the form of a BIST module BIST, a test result memory formed in the example considered by a register block REGB, a number of interface circuits IPCT, and input terminals, formed by pads, as they are known, for the supply of an external clock signal EXTCLK, a first supply voltage Vdd that supplies the integrated circuit with power, with the exception of the register block REGB, a second supply voltage VddR that supplies only the register block REGB with power, a control signal RST_N that controls the BIST module BIST, a control signal ITESTMODE that controls the BIST module BIST and the register block REGB, and a control signal RSTREG_N that controls the register block REGB, it being possible for the terminal for the external clock signal EXTCLK to be dispensed with if the integrated circuit has an internal clock signal generator CLKGEN, which may be the case here.

The BIST module BIST

- is supplied with power by the first supply voltage Vdd already mentioned,

- is clocked by a clock signal CLK generated by the internal clock signal generator CLKGEN,

- receives the control signals ITESTMODE and RST_N already mentioned from outside the integrated circuit,

- receives from the register block REGB a control signal READY, and data Q2 to Q5, and

- outputs to the register block REGB a control signal STROBE, and data D2 to D5.

The register block REGB

- is supplied with power by the second supply voltage VddR already mentioned,

- is clocked by a clock signal CLK generated by the internal clock signal generator CLKGEN,

- receives the control signals ITESTMODE and RSTREG_N already mentioned from outside the integrated circuit,

- receives from the BIST module BIST the control signal STROBE and the data D2 to D5,

- outputs to the BIST module BIST the control signal READY and the data Q2 to Q5, and

- outputs a control signal CLKOFF to the internal clock signal generator CLKGEN or a device that can exert an influence on the external clock signal EXTCLK.

The construction of the register block REGB is shown in figure 2. The register block REGB in the example considered contains

- a number of registers (five in the example considered) DREG1 to DREG5,

- AND elements AND1 to AND3, and

- an inverter INV.

Of the registers DREG1 to DREG5, each contains a data input terminal, a data output terminal Q, a reset terminal R and a clock terminal C,

- the output signal from the first AND element AND1 being input to the data input terminal D of the register DREG1,

- the data D2 to D5 being input to the data input terminal D of the registers DREG2 to DREG5,

- the data item Q1 (used as the READY signal) being output from the data output terminal Q of the register DREG1,

- the data Q2 to Q5 being output from the data output terminals Q of the registers DREG2 to DREG5,

- the signal RSTREG_N being applied to the reset terminals R of the registers DREG1 to DREG5,

- the output signal from the third AND element AND3 being applied to the clock terminals C of the registers DREG1 to DREG5,

- the first AND element AND1 forming an AND combination of the data Q2 and Q3 output from the output terminals Q of the registers DREG2 and DREG3,

- the second AND element AND2 generating an AND combination of the signals READY and ITESTMODE and generating a signal CLKOFF, and

- the third AND element AND3 forming an AND combination of the signals CLK, STROBE and inverted READY.

The interface circuits IPCT already mentioned are connected upstream of the input terminals of the register block REGB for the signals generated within the integrated circuit, that is to say for the signals CLK, STROBE, D2, D3, D4 and D5. Their task is to ensure that the aforementioned signals assume defined states or waveforms when the devices that generate the signals are deactivated, which is the case in particular, as will be explained in more detail later, when the supply voltage Vdd supplying these devices with power is switched off; the aforementioned signals must not float.

Two options for the practical implementation of such interface circuits are shown in figure 3A and figure 3B. These circuits ensure that defined potentials, more precisely VddR or 0 V, are supplied to the register block REGB both when the supply voltage Vdd is applied and when the supply voltage Vdd is switched off.

The interface circuits IPCT shown in figures 3A and 3B differ "only" in the construction of the input stage of the same; however, this has no influence on their function and mode of action.

The interface circuits IPCT shown in figures 3A and 3B function as follows:

When the supply voltage Vdd (=VddR) is applied, the signal present on an input terminal IN is transmitted in inverted form to a junction K and onward from the latter, via a transistor N3, to a Schmitt trigger ST which, depending on the potential of the signal supplied to it (and therefore also depending on the signal supplied to the input terminal IN of the interface circuit IPCT), outputs VddR or 0 V, and whose output signal OUT is at the same time the output signal from the respective interface circuit IPCT.

When Vdd is switched off, the transistor N3 turns off, and the voltage VddR is fed to the Schmitt trigger ST via a transistor P3, as a result of which, irrespective of the signal supplied to the input terminal IN of the interface circuit IPCT, VddR is output from the Schmitt trigger ST and the interface circuit IPCT.

The testing of the integrated circuit by the BIST module BIST proceeds as follows:

At the start of the test, both supply voltages Vdd and VddR and control signals ITESTMODE=1, RST_N=0 and RSTREG_N=0 are applied,

- RST_N=0 resetting the BIST module BIST,

- RSTREG_N=0 resetting the registers DREG1 to DREG5, and

- ITESTMODE=1 causing the BIST module (after the latter has been reset) to test the integrated circuit.

After the expiry of a time, within which the BIST module BIST and the registers DREG1 to DREG5 are reliably reset by the

signals RST_N=0 and RSTREG_N=0, the signals RST_N and RSTREG_N are set to the value 1.

When the test of the integrated circuit carried out by the BIST module in response to the signal ITESTMODE=1 is concluded, the BIST module transmits

- data representing the test result, and

- data representing the test status

to the register block REGB.

In the example considered, two individual tests are carried out by the BIST module, and test result data and an item of test status data are generated for each individual test, these items of data each comprising one bit, and

- test result data with the value 0 indicating that the relevant test was not passed,

- test result data with the value 1 indicating that the relevant test was passed successfully,

- test status data with the value 0 indicating that the relevant test has not yet finished, and

- test status data with the value 1 indicating that the relevant test has finished.

In the example considered, the test result data are the data D4 and D5, and the test status data are the data D2 and D3.

Reference should already be made at this point to the fact that the BIST module BIST can in principle carry out an arbitrary number of individual tests, and that the data about the tests output to the register block REGB can in principle be any desired amount of data, of any desired length, encoded in any desired way and representing any desired information.

The data output by the BIST module BIST to the register block REGB, if the STROBE signal already mentioned, more precisely STROBE=1, is output by the BIST module BIST at the same time, are taken into the registers D2 to D5 and stored in the latter with the respective next rising edge of the clock signal CLK. Via the STROBE signal, the BIST module BIST can exert an influence relating to whether and, if appropriate, when data are stored in the register block REGB. This makes it impossible for the wrong data to be mistakenly written in the register block, and makes it possible for the power consumption in the register block not to be higher than absolutely necessary.

When the BIST module BIST has finally carried out the two individual tests to be carried out by it, in each case the value 1 is present in the registers DREG2 and DREG3. The contents of these registers are subjected to an AND combination by the first AND element AND1, and the result of this AND combination is written to the register DREG1. The value stored in the register DREG1 therefore indicates whether the BIST module BIST has finally carried out all the individual tests to be carried out by it; a DREG content of 0 indicates that the tests have not yet all finally been carried out, and a DREG content of 1 indicates that all the tests have been carried out.

The content of the register DREG1, which can be tapped off on the output terminal Q of the same, is the READY signal which has already been mentioned and which is output from the register block REGB to the BIST module BIST.

The READY signal also controls the value of the signal CLKOFF, and whether the clock terminals C of the registers DREG1 to DREG5 are supplied with a clock signal.

The signal CLKOFF is the result of the AND combination, formed by the AND element AND2, of the signals READY and ITESTMODE, and whether the clock terminals of the registers DREG1 to DREG5 are supplied with a clock signal depends on the result of the AND combination, formed by the AND element AND3, of the negated READY signal and the signals STROBE and CLK.

The signal CLKOFF becomes 1 when the integrated circuit is in the test operating mode (ITESTMODE=1) and the test to be carried out by the BIST module has been completed (READY=1), and is used for the purpose of preventing the clock signal CLK being supplied to the register block REGB and to the remaining components of the integrated circuit. As a result, after the completion of the test to be carried out by the BIST module, the integrated circuit can automatically be put into a state in which it exhibits a minimal power consumption.

It is even better if, additionally or alternatively, CLKOFF=1 is used for the purpose of automatically switching off the supply of the supply voltage Vdd, by means of which the integrated circuit is supplied with power, with the exception of the registered block REGB. One possibility for the practical implementation of this is for an output terminal belonging to the integrated circuit (a pad) to be provided for the signal CLKOFF, and for a switch provided outside the

integrated circuit in the Vdd path and, for example, formed by a transistor, to be operated by the signal output via this pad. Another possibility for switching off the supply voltage is illustrated in figure 4. In the integrated circuit illustrated in figure 4, the switch by means of which Vdd is connected or disconnected is formed by a transistor T provided within the integrated circuit and controlled by CLKOFF. This has the positive effect that the integrated circuit only has to be supplied with a single supply voltage (VddR in the example considered) from the outside; this single supply voltage is supplied both to the register block and - via the transistor T - to the remainder of the integrated circuit, designated by ROC.

Interrupting the supply of Vdd at times during which the integrated circuit has nothing else to do than to ensure that the data stored in the register block REGB are not lost, which, for example, is the case between the end of the test carried out by the BIST module and reaching the external testing device continuing the test of the integrated circuit, proves to be advantageous since, as a result, the power consumption of the integrated circuit can be reduced, which is of great importance in particular when the test carried out by the BIST module is carried out simultaneously for all the integrated circuits on one or more wafers.

The fact that, as has already been mentioned above, the clock terminals C of the registers DREG1 to DREG5 have a signal applied to them which is the result of an AND combination of the signals CLK, STROBE and the inverted signal READY, has the positive effect

- that, in the registers DREG1 to DREG5, it is possible to write only data when the BIST module permits this by outputting STROBE=1, and

- that the writing of data into the registers DREG1 to DREG5 is automatically prevented when the tests to be carried out by the BIST module have been concluded.

The possibilities

- that the register block REGB can be kept in operation while the rest of the integrated circuit is deactivated or switched off, and

- that, by means of the self-locking mechanism described above, it is ensured that the results of the tests carried out by the BIST module, which are stored in the register block REGB, can no longer be overwritten under any circumstances after the conclusion of the test

provide ideal preconditions for permitting the data stored in the register block REGB to be read out and evaluated at any desired time after the end of the test.

In order to read out the data stored in the register block REGB and output said data from the integrated circuit (for example to the external testing device), ITESTMODE=0 and RST_N=0 are set; the signal RSTREG_N remains at the value 1.

Changing the signal ITESTMODE to the value 0 has the effect that the signal CLKOFF, generated on the basis of the former, likewise assumes the value 0. This has the effect that, in turn, the entire integrated circuit is supplied with power, and/or that the clock signal CLK is generated again (in the

case of an internal clock generator) or is forwarded (in the case of an external clock generator).

Since the signal READY maintains the value 1 during this process, the registers DREG1 to DREG5 can still not be written, however.

The BIST module is reset by the signal RST_N=0. The signal RST_N is set to the value 1 again at a time at which it can be assumed that the BIST module has been reset. After that, it is possible to arrange for the integrated circuit to read out the data stored in the register block REGB and to output these data (data Q2 to Q5).

The processes described above are illustrated in figure 5, which shows the waveforms of Vdd, VddR, ITESTMODE, RST_N, RSTREG_N, READY and CLKOFF. Of the times marked in figure 5,

t1 designates the time at which the integrated circuit is started up,

t2 designates the time at which resetting of the integrated circuit has been concluded and the test of the integrated circuit by the BIST module begins,

t3 designates the time at which the self test has been concluded,

t4 designates the time at which Vdd is switched off,

t5 designates the time at which preparations to read out the test result memory are begun,

t6 designates the time at which Vdd is switched on again, and

t7 designates the time at which the reading of the test result memory can be started.

As can be seen from the above explanations, contact has to be made with only a very few input and/or output terminals on the integrated circuit in order to test the integrated circuit by means of the BIST module contained in the latter. The number of input and/or output terminals with which contact has to be made can even be reduced still further if the reset signals RST_N and RSTREG_N are generated within the integrated circuit on the basis of the waveform of the supply voltages Vdd and VddR. A circuit by means of which this can be brought about, for example, is shown in figure 6 and comprises a resistor RST-R, a capacitor RST-C and a Schmitt trigger ST. If use is made of this option, then the input terminals (pads) provided for the signals RST_N and RSTREG_N on the integrated circuit can be dispensed with and, in order to test the integrated circuit by means of the BIST module contained therein, contact has to be made with still fewer input and/or output terminals of the integrated circuit than is already the case anyway.

The supply of power to the register block REGB, provided via the supply voltage VddR, is maintained uninterruptedly at least until the integrated circuit is connected to the external testing device and until the data stored in the register block are read out by means of the external testing device. The voltage source which supplies the supply voltage VddR and/or the contact-making elements via which the supply voltage VddR is applied to the integrated circuit may change, however; this is virtually inevitable, for example, when the integrated circuit is taken by a transport device that transports it to the external testing device, in order to be transported onward by a different transport device, or in

order to be stored temporarily, or in order to be connected to the testing device. In cases in which this is too complicated or impossible, the supply of the integrated circuit with the supply voltage VddR can be provided by a battery connected to the integrated circuit and carried along with the latter, or by a capacitor. This will be discussed in more detail later.

Furthermore, it must of course be ensured that the integrated circuit is supplied with the control signals RST_N, RSTREG_N and ITESTMODE and, if necessary, the clock signal CLK, during the test carried out by the BIST module. This can be done by means of a very simply constructed control device which, in the case in which the test is carried out while the integrated circuit is being transported to the external testing device, is preferably a control device which can be carried along with the integrated circuit, at least during the test.

The test to be carried out by the BIST module is preferably carried out simultaneously in a plurality of integrated circuits, for example in all the integrated circuits belonging to one or more wafers.

The simultaneous performance of the test to be carried out by the BIST module in all the integrated circuits belonging to a wafer may be implemented particularly simply in the case of a wafer as described below.

A wafer of this type is distinguished, inter alia, by the fact that, of the integrated circuits produced on it, at least those points on the integrated circuits to which the voltages and signals required for testing the same by means of the BIST modules have to be supplied are connected electrically to one another.

One such wafer is illustrated in figure 7. In this case, the wafer is designated by the reference symbol W, the integrated circuits produced on it are designated by the reference symbol IC, and the electrical connections between the integrated circuits IC are designated by the reference symbol OVA. In the example considered, the electrical connections OVA interconnect the points on the integrated circuits to which the supply voltages Vdd and VddR, the ground potential GND and the signals RST_N, RSTREG_N and ITESTMODE have to be supplied.

In the example considered, the electrical connections OVA are formed by line sections leading out from the integrated circuits IC, projecting into the interspaces present between adjacent integrated circuits IC and there overlapping with the respectively associated line sections of the adjacent integrated circuits. Such line sections lead away from a plurality of sides, preferably from all four sides of the integrated circuit, the line sections leading away from the various sides of the integrated circuit being interconnected by means of lines running inside or outside the integrated circuit. Such an integrated circuit is illustrated by way of example in figure 8; in this case, the line sections provided to form the connections OVA are designated by the reference symbol OVAP, and the lines connecting these are designated by the reference symbol OVAC. At this point, reference should already be made to the fact that the lines OVAC that connect the line sections OVAP to one another can also have any other desired course and can also run outside the integrated circuits (in the interspaces present between adjacent integrated circuits). In the example considered, the lines OVAC that connect the line sections OVAP to one another are a constituent part of one of the conductive layers of the integrated circuit, that is to say, for example, consist of AlSiCu or of Cu sheathed with Ti or Ti/N.

In the example considered, the line sections OVAP extending beyond the integrated circuits (into the interspaces, also referred to as the snap frame, between adjacent integrated circuits) are produced together with the integrated circuits; in the operations during which the line sections OVAP are produced, masks (reticules) are used which cover a region going beyond the edge of the integrated circuit to be produced.

The integrated circuits belonging to a wafer are produced in a large number of successive steps (deposition, exposure, etching, oxidization, implantation, lithography steps etc.), but with not every step normally being carried out simultaneously for all the integrated circuits; specific steps, for example the exposure of a resist, are carried out individually and successively for each integrated circuit or for groups of integrated circuits each containing a plurality of integrated circuits. This can lead to the situation where no proper connections OVA are produced between integrated circuits which are not processed (for example exposed) together. This can have various causes: firstly, it may occur that the mutually associated line sections OVAP of adjacent integrated circuits or of adjacent groups of integrated circuits which are not exposed together do not align with one another and, secondly, it may occur that, at the points at which they overlap, the connections OVA can become narrower or wider locally as a result of double exposure at these points and, as a result, become so narrow that no good connection is produced, or become so wide that adjacent connections OVA come into contact with each other. This can be prevented by a larger spacing being provided between adjacent line sections OVAP than is usual in the technology used, and by the free ends (those that come to lie in the interspace between

adjacent integrated circuits) of the line sections OVAP being designed to be wider than the rest of the line sections. This is illustrated in figure 9. Figure 9 shows line sections OVAP1 and OVAP2 of a first integrated circuit, and line sections OVAP3 and OVAP4 of a second integrated circuit not exposed together with the first integrated circuit. The line sections OVAP1 to OVAP4 have end portions E which are widened as compared with the remainder. As can be seen from figure 9, the line sections OVAP1 and OVAP3 and, respectively, OVAP2 and OVAP4 which are to be brought into contact with one another are properly in contact even when they are not aligned with one another; because of the particularly large spacings between OVAP1 and OVAP2 and, respectively, between OVAP3 and OVAP4, there is no risk either that short circuits will be produced.

In the case of a wafer in which a plurality or all of the integrated circuits formed on it are connected to one another as described or differently, in order to initiate and to carry out the testing by the BIST modules contained in the integrated circuits, it is sufficient for the voltages and signals to be supplied to the latter to be supplied to the wafer only at a single point or at a few points, for example in one of the contact zones designated in figure 7 by the reference symbols C1, C2, C3 and C4.

An arrangement by means of which this can be done is shown in figures 10A and 10B. Figures 10A and 10B show a (wafer) carrier or chuck WT, a wafer W placed on the carrier WT and a (wafer) contact-making device WK, the contact-making device WK comprising a rod KET which can be moved to and fro in the longitudinal direction, contact pins KE fixed to the rod, and a guide device FV for guiding the rod KET carrying the contact pins KE.

The rod KET can be moved up and down together with the pins KE carried by it. When the rod KET is located in the lower position, the pins KE come into contact with the contact points formed in the contact zone with which contact is made (in one of the contact zones C1 to C4), which contact points can be formed by the line sections OVAP (preferably by the broadened end portions E of the same) present in the relevant contact zone; in the position in which the rod KET is shifted upward, there is no contact between the pins KE and the wafer.

The fact that the wafer has a plurality of contact zones C1 to C4 (four in the example considered but possibly also more or fewer), by which in each case all the integrated circuits IC provided on the wafer can be supplied with the voltages and signals needed for testing the same by means of the BIST modules contained therein, means that the supply of the voltages and signals can then be maintained even if the wafer - for whatever reason - has to be removed from the carrier carrying it.

One possible way of removing the wafer W from the carrier WT while uninterruptedly maintaining the supply of the aforementioned voltages and signals to the integrated circuits is illustrated schematically in figures 11A to 11C. The device that removes the wafer W from the wafer carrier WT in the example considered is a fork F, whose prongs FZ can be inserted from the side of the carrier WT into associated slot-like recesses WTS in the carrier WT and can pull the wafer W away from the carrier WT whilst lifting said wafer slightly. Figure 11A shows the state in which the wafer W is still on the carrier WT and is still being supplied with the voltages and signals needed by the integrated circuits via the contact zone C2. Figure 11B shows the state in which the fork F has

been pushed into the wafer carrier. At this stage, the wafer initially continues to be supplied with the voltages and signals needed by the integrated circuits via the contact zone C2. After the fork F has reached a specific relative position in relation to the wafer W (or the carrier WT carrying the latter), the contact points provided in the contact zone C1 of the wafer W have contact made with them by a contact-making device which is not shown in the figures but is arranged on the fork F, as a result of which the integrated circuits provided on the wafer are then also supplied with the voltages and signals needed by them via the contact zone C1. After this has been done, the supply of the voltages and signals needed by the integrated circuits via the contact zone C2 is interrupted by detecting the appropriate electrical connections. As has already been indicated, interrupting this connection does not result in the integrated circuits no longer receiving the voltages and signals needed by them; these have been and are certainly still supplied via the contact zone C1. After that, the wafer W can be lifted slightly by the fork F and drawn away from the carrier WT together with the said fork; this is illustrated in figure 11C.

Removing the wafer W as described from the wafer carrier WT is preferably carried out at a time at which the test of the integrated circuits to be carried out by the BIST module has already been completed. It is then necessary for the integrated circuits still to be supplied "only" with the supply voltage VddR via the fork F and the contact zone C1. This can be effected, for example, by means of a battery or a capacitor, which is provided in the device that removes the wafer W from the wafer carrier WT; if a capacitor were used, provision could be made to charge this up during the time during which contact is made with the wafer both via the

contact zone C1 and via the contact zone C2, by means of the power supplied to the wafer via the contact zone C2.

It would also be conceivable to supply the wafer with the supply voltages Vdd and/or VddR via a battery permanently connected to the wafer or a capacitor permanently connected to the wafer. Under certain circumstances, this dispenses with the necessity of making contact with the wafer, as the latter is removed from the wafer carrier, via a contact-making device provided on the removal device.

Provision can also be made to test the integrated circuits of a plurality of wafers simultaneously. This is possible, for example, by means of a test box TB shown in figure 12. The test box TB shown contains a housing G and a plurality of wafer carriers WT1 to WTn which are arranged one above another and which are constructed in the same way as or similarly to the wafer carrier WT described with reference to figures 10 and 11. In particular, each wafer carrier contains a contact-making device WK, the contact-making devices of all the wafer carriers being connected to a common control device CM that provides and generates the necessary voltages and signals. The control device CM is either transported together with the text box, or is connected to the contact-making devices WK via lines which are so long that the test box TB and the control device CM can be moved relative to each other. The simultaneous testing of the integrated circuits produced on a plurality of wafers makes it possible to reduce to a minimum the number of control devices CM to be provided for this purpose.

It should be clear that the simultaneous testing of the integrated circuits of a plurality of wafers can also be carried out in a different way than by means of the test box

TB described above. One possibility for this is illustrated in figure 13. In the arrangement illustrated in figure 13, the wafer carriers WT1 ... WTn are arranged one beside another on a disk S that can be rotated about an axis A. The wafer carriers WT1 ... WTn are once again constructed in the same way as or in a similar way to the wafer carriers WT described with reference to figures 10 and 11. Arranged beside the rotating disk S is an external testing device ET. Each time a wafer carrier WT with a wafer W located on it runs past the external testing device ET, the disk S is stopped and

- the integrated circuits IC on the wafer W are tested,

- the wafer W whose integrated circuits have previously been tested are removed from the wafer carrier WT carrying these, and

- the next wafer is placed on the wafer carrier from which the wafer was removed, and

- a start is made, immediately or later, with testing the newly added wafer.

Such an arrangement has the advantage that, during the entire test process of the integrated circuits provided on the wafer, the wafers can remain lying on the wafer carriers WT1 to WTn and do not have to be moved around in between times.

It should be clear that the device carrying the wafer carrier may also be a conveyor belt or any other desired transport device by means of which the wafer carriers, with the wafers arranged on them, can be conveyed to the external testing device.

Given appropriate modification, the method of testing integrated circuits described above can also be employed in the case of semiconductor chips containing integrated circuits and in the case of components containing semiconductor chips.

An arrangement by means of which components containing semiconductor chips can be tested is illustrated in figure 14.

The arrangement shown in figure 14 comprises a component carrier BTT carrying a large number of components BT to be tested, and a control device CM, which ensures that testing of the components by means of the BIST modules contained in them (in the integrated circuits of the same) is at least begun before they are connected to an external testing device (for the purpose of evaluating the self-test results and/or for continued testing). The control device CM supplies the components with the voltages and signals which are needed to initiate and carry out the testing of the same by means of the BIST modules present in them, that is to say, for example, Vdd, VddR, GND, RST_N, RSTREG_N and ITESTMODE. The components are driven, at least partially, in parallel, as a result of which in each case a plurality of components BT or all of the components BT on the component carrier BTT can be tested simultaneously by the BIST modules contained in them.

The arrangement of the components BT on the component carrier BTT is preferably carried out by means of an intermediate carrier which carries the components and can be placed on the component carrier BTT and which (together with the components) can be removed from the component carrier in such a way that the supply of the voltages and signals which must be supplied to the components at the relevant time is not interrupted. An exemplary embodiment of such an intermediate carrier is shown in figures 15A and 15B. The intermediate carrier shown in

figures 15A and 15B and designated by the reference signal ZT is a carrier plate TP having pins P running through it. The component BT is placed on the intermediate carrier ZT and fixed in such a way that the component terminals which are needed for testing the component by means of the BIST module and the external testing device are connected electrically to respectively associated pins. A component placed on such an intermediate carrier is optionally able to be supplied with the voltages and signals which have to be supplied to it for testing by means of the BIST module via the pin parts PU running underneath the carrier plate TP or via the pin parts PO running above the carrier plate TP, the supply being carried out via the lower pin parts PU when and as long as the intermediate carrier ZT is placed on the carrier plate TP, and the supply being carried out via the upper pin parts PO when the intermediate carrier ZT is removed from the carrier plate TP (for example in order to be connected to the external testing device that continues the component test).

Semiconductor chips can also be tested in a similar way.

The method and devices described make it possible to test integrated circuits rapidly and simply, irrespective of the details of the practical implementation.

Patent claims

1. A method of testing an integrated circuit, using a self-test device contained in the latter, wherein the testing of the integrated circuit (IC) by the self-test device (BIST) is begun before the integrated circuit is connected to an external testing device (ET) that reads out and/or evaluates the results of the self test.

2. The method as claimed in claim 1, wherein the testing of the integrated circuit (IC) by the self-test device (BIST) is begun in such good time that the self test has been concluded before the integrated circuit is connected to the external testing device (ET) that reads out and/or evaluates the results of the self test.

3. The method as claimed in claim 1 or 2, wherein the testing of the integrated circuit (IC) by the self-test device (BIST) is carried out, at least to some extent, during temporary storage of the integrated circuit and/or during the transport of the integrated circuit to the external testing device (ET) that reads out and/or evaluates the results of the self test.

4. The method as claimed in claim 3, wherein a self-test control device (CM) that causes the testing of the integrated circuit (IC) by the self-test device (BIST) is moved together with the integrated circuit to be tested.

5. The method as claimed in one of the preceding claims, wherein at least parts of the integrated circuit (IC) are taken out of operation after the same have been tested by the self-test device (BIST).

6. The method as claimed in claim 5, wherein, after the testing of the integrated circuit (IC) by the self-test device (BIST), the components of the integrated circuit which are not needed in order to continue to store data stored in a test result memory (REGB) written by the self-test device are taken out of operation.

7. The method as claimed in claim 5 or 6, wherein the action of taking the integrated circuit (IC) out of operation comprises preventing the supply of a clock signal (CLK) needed to operate the integrated circuit to individual, a plurality of or all the components of the integrated circuit.

8. The method as claimed in one of claims 5 to 7, wherein the action of taking the integrated circuit (IC) out of operation comprises preventing the supply of a supply voltage (Vdd) that supplies the integrated circuit with power to individual or a plurality of components of the integrated circuit.

9. The method as claimed in one of the preceding claims, wherein the testing of the integrated circuit (IC) by the self-test device (BIST) is carried out simultaneously for a large number of integrated circuits.

10. The method as claimed in claim 9, wherein the testing of the integrated circuit (IC) by the self-test device (BIST) is carried out simultaneously for all the integrated circuits of one or more wafers (W).

11. A device for testing an integrated circuit, using a self-test device contained in the latter, wherein a self-test control device (CM) is provided which causes the testing of the integrated circuit (IC) by the self-test device (BIST) before the integrated circuit is connected to an external

testing device (ET) that reads out and/or evaluates the results of the self test.

12. The device as claimed in claim 11, wherein the self-test control device (CM) causes the testing of the integrated circuit (IC) by the self-test device (BIST) in such good time that the self test is concluded before the integrated circuit is connected to the external testing device (ET) that reads out and/or evaluates the results of the self test.

13. The device as claimed in claim 11 or 12, wherein the self-test control device (CM) permits the testing of the integrated circuit (IC) by the self-test device (BIST) to be carried out, at least to some extent, during temporary storage of the integrated circuit and/or during the transport of the integrated circuit to the external testing device (ET) that reads out and/or evaluates the results of the self test.

14. The device as claimed in one of claims 11 to 13, wherein the self-test control device (CM) is a device that can be moved together with the integrated circuit (IC) to be tested.

15. The device as claimed in one of claims 11 to 14, wherein the external testing device (ET) that reads out and/or evaluates the results of the self test is a testing device by means of which components or functions of the integrated circuit (IC) that are not tested by the self-test device (BIST) are tested.

16. An integrated circuit with a self-test device, wherein the integrated circuit (IC) contains means which make it possible to arrange that, during the testing and/or after the testing of the integrated circuit (IC) by the self-test device

(BIST), specific parts of the integrated circuit are taken out of operation.

17. The integrated circuit as claimed in claim 16, wherein the integrated circuit (IC) contains means which make it possible to arrange that, after the testing of the integrated circuit by the self-test device (BIST), the components of the integrated circuit which are not needed in order to continue to store data stored in a test result memory (REGB) written by the self-test device are taken out of operation.

18. The integrated circuit as claimed in claim 16 or 17, wherein the integrated circuit (IC) contains means which make it possible to arrange that, during the testing and/or after the testing of the integrated circuit by the self-test device (BIST), the supply of a clock signal (CLK) needed to operate the integrated circuit to individual, a plurality of or all components of the integrated circuit is prevented.

19. The integrated circuit as claimed in one of claims 16 to 18, wherein the integrated circuit (IC) contains means which make it possible to arrange that, during the testing and/or after the testing of the integrated circuit by the self-test device (BIST), the supply of a supply voltage (Vdd) that supplies the integrated circuit with power to individual or a plurality of components of the integrated circuit is prevented.

20. The integrated circuit as claimed in one of claims 16 to 19, wherein the integrated circuit (IC) contains means which make it possible to arrange that the content of a test result memory (REGB) that is written by the self-test device (BIST) can no longer be changed after the testing of the integrated circuit by the self-test device.

21. The integrated circuit as claimed in one of claims 16 to 20, wherein the integrated circuit (IC) contains means which make it possible, by using data stored in a test result memory (REGB) that is written by the self-test device (BIST), to detect whether the test to be carried out by the self-test device has been completed or not.

22. The integrated circuit as claimed in one of claims 16 to 23, wherein the integrated circuit (IC) is constructed in such a way that the voltages and signals which have to be supplied to it in order that it can be tested by the self-test device (BIST) contained in it can in each case be supplied to it via at least two different points (C1 to C4).

23. The integrated circuit as claimed in claim 22, wherein the at least two different points (C1 to C4) are connected to one another electrically.

24. A wafer with a large number of integrated circuits, wherein integrated circuits (IC) to be separated later by cutting up the wafer (W) are at least partially electrically connected to one another.

25. The wafer as claimed in claim 24, wherein the electrical connections (OVA) that connect the integrated circuits (IC) are formed by conductor tracks (OVAP) formed on the wafer (W).

26. The wafer as claimed in claim 24 or 25, wherein the electrical connections (OVA) that connect the integrated circuits (IC) in each case connect together those points on the integrated circuits to which specific voltages and/or signals must be supplied in order to test the integrated

circuits by means of a self-test device (BIST) contained in them.

27. The wafer as claimed in one of claims 24 to 26, wherein the wafer (W) contains contact zones (C1 to C4) which are arranged and constructed in such a way that voltages and signals applied to them can be led onward, via the electrical connections (OVA) that connect the integrated circuits (IC) to one another, to a plurality of or all the integrated circuits on the wafer.

28. The wafer as claimed in claim 27, wherein the integrated circuits (IC) can be fed with the voltages and signals which have to be fed to the integrated circuits in order that they can be tested by a self-test device (BIST) contained in them via at least two different contact zones (C1 to C4).

Abstract

Method and device for testing an integrated circuit, integrated circuit to be tested, and wafer with a large number of integrated circuits to be tested

The method described and the device described for testing an integrated circuit are defined by the fact that the testing of the integrated circuit to be tested is begun by a self-test device contained in it before the integrated circuit is connected to an external testing device that reads out and/or evaluates the results of the self test. The integrated circuit and the wafer are constructed in such a way that this is readily possible with little outlay.

List of reference symbols

A	Axis of rotation of S
ANDx	AND elements
BIST	Built-In Self-Test Module in IC
C	Clock terminal of DREG
CLK	Clock signal
CLKGEN	Internal clock signal generator in IC
CLKOFF	Control signal in IC
CM	Control device
DREGx	Register of REGB
D	Data input terminal of DREG
D2-D5	Data representing the test result of the self test
E	Widened end portion of OVAP
ET	External testing device
EXTCLK	External clock signal for IC
F	Fork
FV	Guide device for KET
FZ	Prongs of F
G	Housing of TB
IC	Integrated circuit
IN	Input terminal of IPCT
INV	Inverter
IPCT	Interface circuit in IC
ITESTMODE	Control signal for IC
K	Junction in IPCT
KE	Contact pins of WK
KET	Rod of WK
Nx	NMOS transistors
OUT	Output signal from IPCT
OVA	Connections between ICs
OVAC	The OVAs of lines connecting an IC
OVAPx	Line sections for producing the OVAs
Q	Data output terminal of DREG

P	Pins of TP
Px	PMOS transistors
PO	Upper part of P
PU	Lower part of P
Q2-Q5	Data representing the test result of the self test
R	Reset terminal of DREG
READY	Control signal in IC
REGB	Test result memory in IC
REGRST_N	Control signal for IC
ROC	Rest of IC
RST-C	Capacitor
RST_N	Control signal for IC
RST-R	Resistor
S	Disk
ST	Schmitt trigger
STROBE	Control signal in IC
T	Transistor
TP	Carrier plate
TB	Test box
Vdd	First supply voltage for IC
VddR	Second supply voltage for IC
W	Wafer
WK	Wafer contact-making device
WTx	Wafer carrier
WTS	Recesses in WT
ZT	Intermediate carrier